

High frequency positive series resistance in IMPATT devices

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A generalized computer method, which considers drift, diffusion and tunnel currents has been formulated and used to determine the high frequency series resistance (R_s) and its distribution profile along the active layer of a varieties of Avalanche Transit Time (ATT) diode structures. The method is also capable of providing RF properties of the diodes like RF negative resistance (Z_R), band width and mean square noise voltage $\langle V^2 \rangle / df$ and other parameters at various frequencies. The result indicates generation of high value of R_s , Z_R and $\langle V^2 \rangle / df$ for lo-hi-lo and hi-lo double drift region (DDR) diodes as compared to flat profile diodes. A comparison of the series resistance (R_s), microwave properties and noise generation of Si, GaAs and InP DDR diodes has also been made in this paper. The R_s distribution profiles for the hi-lo and lo-hi-lo DDRs are observed to have double spike like profile unlike the normal double peak profiles for flat DDRs.

The IMPATT (IMPact Ionization and Avalanche Transit Time) diodes are the premier devices in generating mm-wave and microwave power over a wide range of frequencies (10 to 360 GHz). These devices are versatile as regards to base materials and diode structures. The IMPATT diodes are basically reverse-biased p - n junctions that operate under avalanche breakdown condition. The p - n junction under avalanche breakdown condition exhibits high frequency negative resistance in the microwave frequency range. In fact, the negative resistance is produced by the combined effect of the avalanche buildup of charge carriers due to impact ionization and transit time of charge carriers required to cross the depletion zone of the device.

A number of discrepancies between theoretically predicted and experimentally realized performance of high power and high efficiency ATT devices have been indicated in the reported studies¹. The authors observe that the high frequency series resistance arising mostly due to un-depleted low doped zone could be one of the prominent factors for practically limiting efficiency and power in several cases. Some studies on series resistance of IMPATT diodes are also reported². A method incorporating unequal ionization rate of electrons and holes in silicon has been reported³ to compute the series resistance. Since the series positive resistance in a diode is sensitive to several other physical processes involved in IMPATT action, the authors have developed a generalized computer simulation method to compute the series resistance and other microwave properties of the ATT

devices by considering realistic features like diffusion and tunnel currents, mobile space charge effect and realistic variation of the material parameters in the semiconductors^{4,5}. The method has been used to compute the series resistance and other properties generated in a variety of diode structures under different operating conditions and with different base materials. The result is in agreement with the earlier reports^{2,3}. The interesting features arising out of the series resistance distribution profile along the depletion zone *vis-à-vis* microwave negative resistance distribution profile has been described. The high value of series resistance in case of lo-hi-lo diodes may be taken as the reason for limiting the microwave performance of these diodes below the predicted theoretical values. The high noise generation in the high efficiency diodes can be taken as another deteriorating performance parameter for the hi-lo and lo-hi-lo diodes.

Numerical Method

Material parameters

The variation of ionization rates with electric field and temperature in silicon has been taken from the work of Grant⁸. Ito *et al.*⁹ and Kao *et al.*¹⁰ have determined the ionization rates for GaAs and InP respectively. The ionization rate in silicon is expressed in an exponential equation of the form,

$$\alpha_{n,p} = A_{n,p} \exp(-b_{n,p}/E),$$

where E is the electric field and $A_{n,p}$ and $b_{n,p}$ are constants which take different values for different

field ranges. The values of these constants for Si (at 22 °C) for different field ranges and for <100> oriented GaAs and InP have been given in Table 1. Grant⁸ has also shown that the ionization rate in Si decreases with increase in temperature. The temperature dependence of α_n and α_p is expressed by making the constants b_n and b_p to vary with temperature as,

$$(b_n)_T = (b_n)_{22} + 1.35 \times 10^5 (T - 22)$$

$$\text{and } (b_p)_T = (b_p)_{22} + 1.1 \times 10^5 (T - 22)$$

where $(b_{n,p})_T$ and $(b_{n,p})_{22}$ are the values of $b_{n,p}$ at $T^\circ\text{C}$ and at 22 °C. The authors have considered these values at 200 °C (junction temperature) for the analysis.

The drift velocities of both electrons and holes in different semiconductors increase with electric field upto a strength of 10^7 V/m and then get saturated. The drift velocities of both electrons and holes are expressed in the form,

$$v_{n,p} = v_{sn,sp} [1 - \exp(-\mu_{n,p} E / v_{sn,sp})]$$

The same exponential form is valid for hole velocities in GaAs and InP. But in case of electrons in GaAs and InP, the drift velocities is expressed by a fourth power velocity ~ field variation which is given in the form,

$$V_n = \{ \mu_n E + V_{s,n} (E / E_C)^4 \} / \{ 1 + (E / E_C)^4 \}$$

where E_C is the electric field corresponding to the peak electron velocity in the velocity ~ field characteristics. Other material parameters like

Table 1 — Ionization rate parameters for Si (at 22 °C) and <100> oriented GaAs and InP for different field ranges

Si				
Field range 10^7 V/m	A_n (10^8 m^{-1})	b_n (10^8 Vm^{-1})	a_p (10^8 m^{-1})	b_p (10^8 Vm^{-1})
2.0 – 2.4	2.6	1.43	2.0	1.97
2.4 – 5.3	0.62	1.08	2.0	1.97
5.3 – 7.7	0.50	0.99	0.56	1.32
GaAs				
2.5 – 7.7	5.6	2.41	1.5	1.57
InP				
3.5 – 6.5	5.55	3.1	1.98	2.29

Table 2 — Other material parameters of Si, GaAs and InP

Material	V_{sn} (10^4) ms^{-1}	μ_n $\text{m}^2\text{V}^{-1}\text{s}^{-1}$	V_{sp} (10^4) ms^{-1}	μ_p $\text{m}^2\text{V}^{-1}\text{s}^{-1}$	E_C (10^6) Vm^{-1}	ϵ (10^{-10}) F/m	E_g (eV)
Si	10.5	0.145	8.1	4.5	-	1.04	1.12
GaAs	8.0	0.85	10.0	0.04	0.65	1.16	1.45
InP	7.5	0.46	7.5	0.015	1.1	1.09	1.42

mobilities (μ), permittivity (ϵ) of the silicon metal and band gap energy (E_g) which are used for the analysis are given in the Table 2.

At first silicon single drift region (SDR) diodes having structural forms n^+pp^+ and n^+np^+ and flat double drift region (DDR) diodes with forms n^+npp^+ and the high efficiency structures like $n^+nn^+npp^+pp^+$ (lo-hi-lo) and $n^+nn^+p^+pp^+$ (hi-lo) have been designed and optimized for operation in mid Ku-band having center frequency around 18 GHz (first atmospheric window frequency) considering appropriate punch through factor (PTF) value. The width of p and n side of the diode is 2.0 μm . The doping and operating current density are taken to be $1.2 \times 10^{22} / \text{m}^3$ and $2 \times 10^7 \text{ A/m}^2$ for flat DDR diode respectively.

These diodes have been analyzed under static conditions through simultaneous solution of the Poisson's equation, carrier continuity equation and space charge equation across the depletion zone of the respective diodes following a double iterative computer method as has been reported^{4,5}. The method incorporates realistic impurity diffusion profile near the junction¹¹, actual variation of material parameters due to electric field and temperature.

DC analysis

The basic equations involved for DC analyses are :

The Poisson's equation

$$dE/dx = (q/\epsilon) (N_D - N_A + p - n) \quad \dots (1)$$

The carrier continuity equations $dn/dt = (1/q) (dJ_n/dx) + (\alpha_n n v_n + \alpha_p p v_p)$ and

$$dp/dt = (-1/q) (dJ_p/dx) + (\alpha_n n v_n + \alpha_p p v_p) \quad \dots (2)$$

Here n and p represents electron and hole concentration, $\alpha_{n,p}$ and $v_{n,p}$ represent ionization rates and carrier velocities for electrons and holes respectively. The respective carrier current densities can be written as $J_p = q p v_p$ and $J_n = q n v_n$ and the total current density is expressed as $J_o = J_n + J_p$

Under static condition the Eq. (2) takes the form,

$$(1/q)(dJ_p/dx) = \alpha_n n v_n + \alpha_p p v_p = -(1/q)(dJ_n/dx) \quad \dots (3)$$

Defining $P(x) = \{J_p(x) - J_n(x)\} / J_o$, the pairs of

Eq. (4) are transformed into,

$$dP(x) / dx = (\alpha_n + \alpha_p) - (\alpha_n - \alpha_p) P(x) \quad \dots (4)$$

and

$$qd(p-n)/dx = -q(\alpha_n - \alpha_p)(p-n) + J_o \{ (\alpha_n / v_p) + (\alpha_p / v_n) \} + (dE/dx)K \quad \dots (5)$$

where the correction factor K is defined as, $K = (J_p) d/dE (1/v_p) - (J_n) d/dE (1/v_n)$

Eqs (1), (4) and (5) are solved taking proper boundary conditions into account. The boundary conditions are obtained as follows :

At left edge of the depletion layer, i.e., at $x = x_L$, the hole current comprises of only the reverse saturation current J_{sp} .

Thus at $x = x_L$,

$$P(x) = (J_p - J_n) / J_o = \{ J_{sp} - (J_o - J_{sp}) \} / J_o = 2 (J_{sp} / J_o) - 1$$

Defining the hole multiplication factor to be $M_p = J_o / J_{sp}$,

one can write, $P(x_L) = (2 / M_p) - 1$

Similarly at the right hand edge of the depletion layer, considering the electron current to be comprising of only the reverse saturation current J_{sn} ,

one can write, $P(x_R) = 1 - (2 / M_n)$, where electron multiplication factor $M_n = J_o / J_{sn}$

It is to be noted here that the field boundary conditions are also to be satisfied at the edges of the depletion zone as $E(x_L) = E(x_R) = 0$

The maximum electric field (E_m) and its location (X_0), drift voltage (V_D), breakdown voltage (V_B), the device efficiency (η) etc have been computed from the static analysis of the diodes following the methods^{4,5}.

Small signal analysis

Taking DC data as input, high frequency small signal analysis of the diodes has been carried out through simultaneous solution of two second order differential equations in diode resistance (R) and reactance (X). The equations are given as,

$$D^2R + (\alpha_n - \alpha_p)DR - (2\omega/v)DX + \{ (\omega^2/v^2) - H(x) \} R - (2\alpha\omega/v)X = 2\alpha/v\epsilon \quad \dots (6)$$

and

$$D^2X + (\alpha_n - \alpha_p)DX + (2\omega/v)DR + \{ (\omega^2/v^2) - H(x) \} X + (2\alpha\omega/v)R = -\omega/v^2\epsilon \quad \dots (7)$$

With $H(x) = (2J_o / v \epsilon)(d\alpha / dE) + (d / dE) (\alpha_p - \alpha_n) D E_m$

The Eqs (6) and (7) are solved simultaneously by the modified Runge-Kutta method within the active layer of the diode with proper boundary conditions⁷ which are given as,

$\epsilon \{ (dR / dx) - (\omega / v_p) . X \} - (1 / v_p) = 0$ and $\{ (dX / dx) + (\omega / v_p) R \} = 0$ at the p -side of the boundary $x = x_R$

$\epsilon \{ (dR / dx) + (\omega / v_n) . X \} + (1 / v_n) = 0$ and $\{ (dX / dx) - (\omega / v_n) R \} = 0$ at the n -side of the boundary $x = x_L$

Iterating over initial choice of initial values of R and X at the left-hand edge (n - side), the boundary conditions on the right hand edge (p -side) are satisfied to give the final solution. The final solution of Eqs (6) and (7) gives RF properties and the spatial distribution of negative resistance R and reactance X . The integrated values of the resistance and reactance are obtained as,

$$Z_R = \int R(x) dx \text{ and } Z_X = \int X(x) dx.$$

The device negative conductance (G) and susceptance (B) are calculated using the relation,

$$G = Z_R / (Z_R^2 + Z_X^2), \quad B = -Z_X / (Z_R^2 + Z_X^2)$$

The small signal analysis is repeated for several frequencies and the optimum frequency (f_p) corresponding to diode peak negative conductance ($-G_p$) where the device gives maximum microwave power is computed in each case.

In addition to the microwave negative resistance, the diode also generates considerate RF positive series resistance. This positive RF series resistance arises from n^+/p^+ substrate, metal semiconductor contact, un-depleted epilayer and device packaging. Thus positive series resistance can be taken as an important parameter which limits the generation of microwave power in the device. The diode positive resistance (R_s) is calculated using the relation⁶, $g = -G - B^2 R_s$, where g is the load conductance. Under small signal condition R_s can be calculated by considering the value of load conductance g to be nearly equal to the diode conductance.

Noise analysis

The random multiplication of charge carriers within the active zone of the device avalanche process generates avalanche noise, which is an unfavourable characteristic of the device. The authors have also

computed the avalanche noise generated in all the diodes following another double iterative computer method.

Taking noise generating source at a particular space point ($x = x'$) within the active layer of the diode, two second order differential equations on the real and imaginary parts of the noise electric have been obtained⁷. These device equations have been solved through the modified Runge-Kutta method with usual boundary conditions at the edges of the diode depletion layer. The final solution of this iterative computer method gives the noise generation profile along the diode active layer for the noise generating source at $x = x'$. Changing the location of this noise source to subsequent points in sequence along the diode active zone, the analysis is repeated. Integration of the results leads to the estimation of the mean squared noise voltage $\langle V^2 \rangle / df$ ⁷.

The methods described above are used to compute DC, microwave and noise properties and series positive resistance of diodes having different doping profiles, structures and materials.

Results and Discussion

The DC and RF characteristics of Silicon n^+np^+ , n^+pp^+ SDR, flat, lo-hi-lo and hi-lo DDR diode structures have been given in Table-3. From the table it is seen that the qualitative value of device efficiency (η) is expected to be 23.7 % for lo-hi-lo structure as against 12.9 for flat diode. The normalized avalanche zone width (x_A/W) ratio becomes only around 10 % for lo-hi-lo DDR and more than 40 % for flat profile DDR. However, when one observes the value of series resistance of different diode structures, it can be seen that the value of R_s for lo-hi-lo DDR is five times higher than that of flat SDR diode. Even the flat DDR diode has the value of $R_s = 0.34 \times 10^{-7} \Omega m^2$ as against

$R_s = 0.1 \times 10^{-7} \Omega m^2$ for flat SDR diode. The R_s profile for DDR diode structure along the active layer of diode is shown in Fig.1. An interesting feature can be seen. The R_s profile shows normal double peak characteristics for flat DDR but double spike-like characteristics are observed for lo-hi-lo and hi-lo DDR diodes. The magnitude of positive resistance peak is higher by several orders of magnitude for lo-hi-lo and hi-lo DDRs compared to that of the flat DDR. However, the positive series comes from very narrow width of the depletion zone for the high efficiency diodes, whereas, in case of the flat DDR almost the entire depletion zone contributes to series resistance. The negative resistance profile, which also exhibits double peak nature, does not show such major differences from structure to structure. When one considers the microwave negative resistance and series resistance together, the net negative resistance

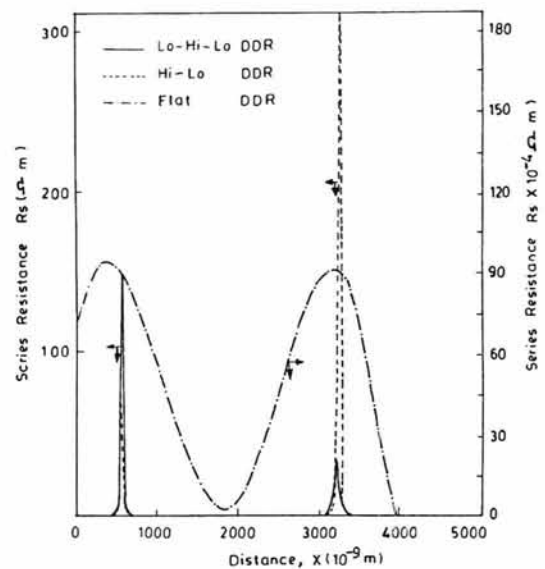


Fig.1 — Variation of series positive resistance of flat, lo-hi-lo and hi-lo DDR structure for Ku-band (18 GHz) operation

Table 3 — DC, microwave and noise properties of different optimized diode structure

Properties	n^+np^+ SDR	n^+pp^+ SDR	Flat DDR	lo-hi-lo DDR	hi-lo DDR
E_m (10^7 V/m)	4.35	4.44	3.86	5.18	6.18
V_B (V)	50.4	55.0	85.4	60.6	68.2
η (%)	7.61	13.5	12.9	23.7	23.2
x_A/W (%)	54.8	40.4	40.5	9.0	11.2
$-G_p$ (10^6 S/m ²)	0.893	1.09	0.708	1.78	1.71
B_p (10^6 S/m ²)	3.66	3.91	1.77	2.29	2.38
f_p (GHz)	18	18	16	21	21
R_s ($10^{-7} \Omega m^2$)	0.100	0.107	0.340	0.510	0.456
$-Z_{Rp}$ ($10^{-7} \Omega m^2$)	0.629	0.662	1.97	2.11	1.99
$\langle V^2 \rangle / df$ (10^{-16} V ² .s)	1.50	1.20	4.84	29.6	29.9

Table 4 — DC, microwave and noise properties of K-band DDR IMPATTs of different material

Properties	Si	InP	GaAs
E_m (10^7 V/m)	4.81	5.64	4.44
V_B (V)	38.9	63.0	61.1
η (%)	11.4	14.0	16.1
x_A/W (%)	43.9	37.0	32.3
$-G_P$ (10^6 S/m ²)	3.22	2.94	3.63
B_P (10^6 S/m ²)	10.5	8.89	5.87
f_P (GHz)	35	35	35
R_s (10^{-8} Ω m ²)	0.436	0.557	1.58
$-Z_{RP}$ (10^{-8} Ω m ²)	2.66	3.35	7.62
$\langle V^2 \rangle / df$ (10^{-17} V ² .s)	4.12	4.77	8.17

for all the three types of DDR diodes (lo-hi-lo/ hi-lo / flat) indicating power generation from all the diodes remains almost the same. Further it can be seen from the table that the mean square noise voltage generated at the optimum frequency of the lo-hi-lo and hi-lo diodes is one order higher than that of the flat diodes. It can therefore be mentioned here that the extent of superior performance, which is predicted on the basis of RF analysis of a lo-hi-lo diode is nullified due to higher series resistance R_s and higher generation of avalanche noise in this diode.

It is further observed that the value of R_s and its profile is predominantly determined by the width, location and impurity concentration of the charge bump of the lo-hi-lo diode structure. Thus one can explore the possibilities of designing lo-hi-lo and hi-lo diodes to give low R_s value.

The Ka-band Si, GaAs and InP DDR flat profile diodes have been also analyzed following the same computer method and the results are presented in the Table 4. This shows that the device efficiency (η) of GaAs is the highest followed successively by InP and Si DDRs. This enhanced efficiency of GaAs IMPATT diode can be explained on the basis of localized avalanche region. GaAs IMPATT diode structure also provides larger value of the diode negative conductance followed successively by Si and InP. However, the series resistance R_s calculated by our simulation method is found to be the highest for GaAs structure and least for that of Si. The distribution of series resistance along the active layer of the diode is shown in Fig. 2. The series resistance profiles show a double peak variation, having the peaks in the central drift region separated by a minimum in the avalanche zone. The magnitude of peak for GaAs (not shown in the figure) is higher by an order of magnitude

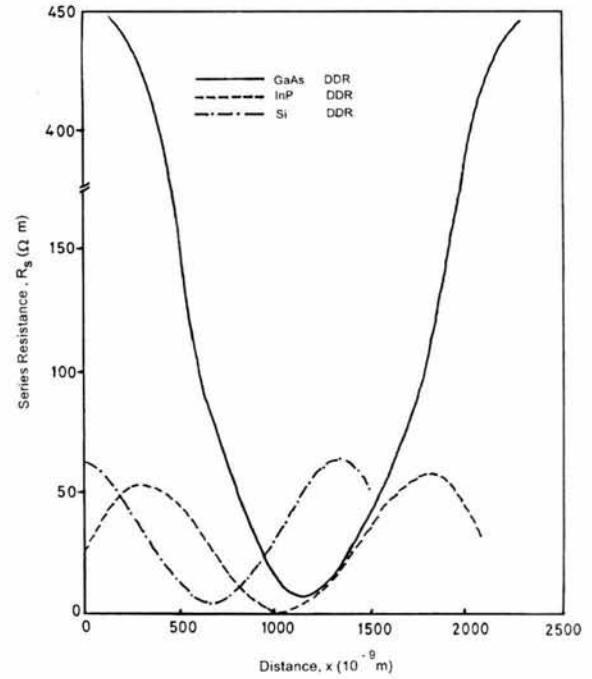


Fig.2 — Variation of series positive resistance of Si, GaAs and InP DDR diodes operated in Ka-band (35 GHz)

compared to that for Si and InP DD diodes, which is responsible for nullifying the advantage for this material due to localized avalanche zone and high microwave negative resistance. The microwave negative resistance profiles of these diodes also show a double peak nature but the magnitude of peaks for Si, GaAs and InP DDRs are of the same order. Amongst Si and InP diodes, it can be seen that the series resistance profiles of InP diode spreads to a higher width of depletion zone compared to that of Si diode. The integrated value of R_s for InP diode is therefore higher compared to that of Si diode, even though the magnitude of the peaks is comparable. However, when one takes into account the high frequency negative resistance together with high frequency positive series resistance, the performance of GaAs DDR diode would remain encouraging compared to corresponding Si and InP DDRs. However, the slight increase in the mean square noise voltage at optimum frequency for GaAs diode would be an unfavorable parameter in its operation. Our investigation shows the similar trend for all other frequency bands of operation.

Conclusion

The series positive resistance and mean square noise voltage of IMPATT diodes with different base materials, different structural parameters and different

operational conditions have been studied. The series positive resistance and mean square noise voltage have been observed to be a prominent limiting factor for the diodes under IMPATT mode of operation. It is interesting to note that for all the cases, the series positive resistance is inversely proportional to the diode susceptance ($R_s = 1/2B$). Thus series resistance can be minimized by proper design of the diode leading to high value of the diode susceptance, which can be achieved by lowering the diode area of cross-section.

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