

## FPGA-based PWM control of hybrid single-phase active power filter for harmonic compensation

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This paper presents implementation of sinusoidal pulse-width-modulation (PWM) for a single-phase hybrid power filter. A series active power filter and a shunt passive filter were combined to suppress harmonic current and isolate harmonic between source and load. For active filter control, PWM was developed in an ALTERA® FLEX 10K Field Programmable Gate Array (FPGA), and modulation index was selected by calculating DC bus voltage of active filter through a digital Proportional-Integral-Derivative (PID) controller. System has been found capable of compensating load current and voltage harmonic within specification of EMC standard IEC 61000-3-2.

**Keywords:** Active filter, PWM, Harmonic compensation, FPGA

### Introduction

Active filter development has resulted from microelectronic revolution, which progressed from discrete analog and digital components to microprocessors, micro-controllers, and digital signal processors (DSPs). Development enables use of control algorithms [proportional integral (PI), variable-structure control, fuzzy logic, and neural network] in improving dynamic and steady state performance of active filters. With such improvement, active filters can provide fast corrective action, even with dynamically changing non-linear loads<sup>1,2</sup>. Harmonic elimination by active power filter depends entirely on modulation method. In order to reduce harmonics, carrier frequency must be raised, but this complicates control circuit and increases switching loss<sup>2</sup>.

Main causes of voltage harmonic distortion are sudden loading of system at common coupling point, large neutral currents due to unbalance loading, improper grounding, etc<sup>3</sup>. These effects result the voltage drop in supply line impedance, generation of earth-neutral volt-

age and interference in communication system. Process control system can often lead to data loss and malfunctioning of protective relay. Primary effects of current waveform distortions are power factor reduction, poor utilization of distribution wiring plant, high current flow in neutral line of four-wire three-phase system and dangerous over heating of cable<sup>4</sup>. These current harmonics result in an increase in the level of rms supply current, power loss, heating of equipment, and increase in reactive power demand.

Most computation resources of a microprocessor's DSP must be devoted to generating pulse-width-modulation (PWM) signals with a high sampling rate. DSP handles PWM generation, while processor feeds DSP-required information. Although this method resolves sampling-rate problems, it complicates the design<sup>5</sup>. Another method is generation of PWM by using field programmable gate array (FPGA), a programmable logic device (PLD), comprising thousands of logic gates. Various FPGA-based digital circuits have been implemented, especially in direct motor control (AC and DC machines), industrial control, power electronics, telecommunication systems, and motion control<sup>6,7</sup>.

Paper presents implementation of sinusoidal PWM for a single-phase hybrid power filter.

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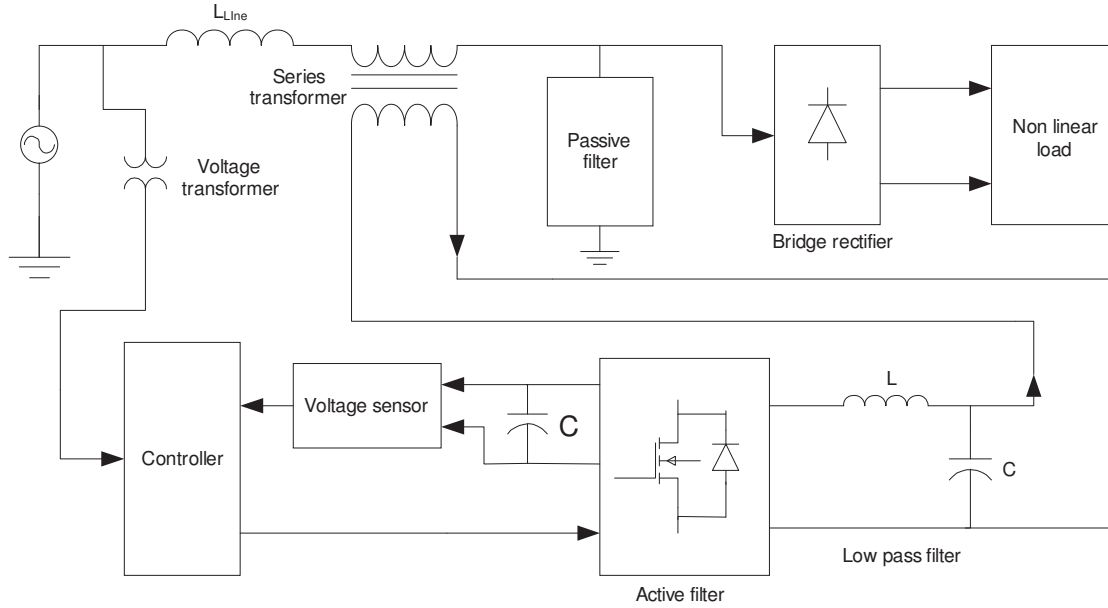


Fig. 1—System configuration of hybrid active power filter

### System Configuration and Analysis

In an active power filter<sup>8</sup> (APF, Fig. 1), a single-phase voltage source inverter is connected in series by a matching transformer between AC source and a single-phase full bridge diode rectifier with a non-linear load. A passive filter is connected in parallel with the load at load end. A low pass (LC) filter passes fundamental component of inverter output voltage to the system through matching transformer, and blocks higher order harmonics. In this configuration, passive filter bypasses current-harmonic component, according to the designed value of passive element. APF acts as a voltage compensator and a harmonic isolator for source and load. Voltage compensation is done by injecting to the line, i.e. the in-phase voltage. Harmonic isolation is also done by the series compensation behaving as active impedance, not causing voltage drop for fundamental component, but forcing current harmonic component to pass through passive filter. Thus, APF improves both filtering characteristics of passive filter and load power factor by compensating reactive power required by the load.

A sinusoidal reference waveform (50 Hz), compared with a triangular carrier waveform, generates gate signals for inverter's switches (Fig. 2). Amplitude of reference waveform is obtained by multiplying a fixed-amplitude sine wave with the amplitude of a variable processed signal, which is key to the inverter's output voltage control. Processed signal is extracted by comparing it with reference DC value and with DC-bus

capacitor voltage. Error signal (difference between DC-bus voltage and DC reference voltage) is processed by a Proportional, Integral, and Derivative (PID) controller for stability<sup>2,9</sup>.

Assume source voltage as

$$V_s(t) = V_m \sin \omega t \quad \dots(1)$$

and non-linear load current is given as

$$i_L(t) = \sum_{n=1}^{\infty} I_n \sin(n\omega t + \phi_n) \quad \dots(2)$$

Total power supplied to load is

$$\begin{aligned} P_L &= V_s(t) * i_L(t) \\ &= I_1 V_m \sin^2(\omega t) \cos \phi_1 + I_1 V_m \sin(\omega t) \cos(\omega t) \sin \phi_1 \\ &\quad + \sum_{n=2}^{\infty} I_n \sin(n\omega t + \phi_n) * V_m \sin(\omega t) \end{aligned} \quad \dots(3)$$

Based on Eq. (3),

$$P_{real} = I_1 V_m \sin^2(\omega t) \cos \phi_1 \quad \dots(4)$$

$$P_{reactive} = I_1 V_m \sin(\omega t) \cos(\omega t) \sin \phi_1 \quad \dots(5)$$

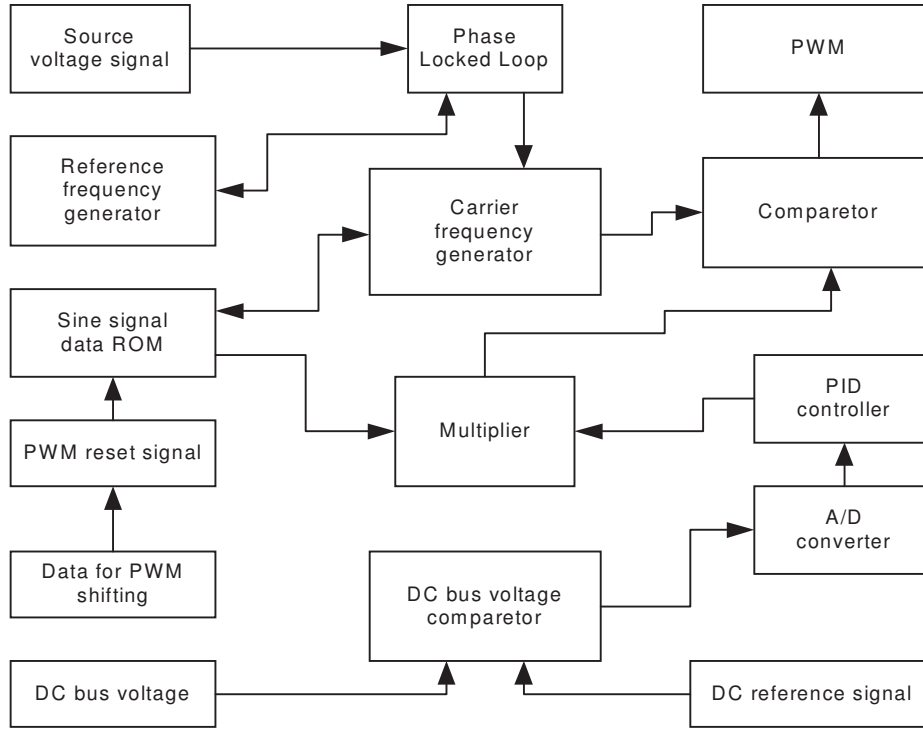


Fig. 2—Block diagram of an active-power-filter control

$$P_{harmonic} = \sum_{n=2}^{\infty} I_n \sin(n\omega t + \varphi_n) * V_m \sin(\omega t) \quad \dots(6)$$

While maintaining DC bus voltage constant, APF provides compensated harmonic voltage and reactive power required by load.

For conventional PWM, amplitude modulation index is given as

$$m = \frac{V_{ref}}{V_{triangle}} \quad \dots(7)$$

where  $V_{ref}$  is amplitude of sinusoidal voltage, and  $V_{triangle}$  is amplitude of triangular carrier voltage. Therefore, output voltage of inverter is

$$V_{out} = m * V_{dc} \quad \dots(8)$$

where  $V_{dc}$  is DC bus voltage of APF.

DC bus capacitor helps in reducing noise. However, in variable non-linear system, active filter DC bus voltage is not constant. Difference between DC bus

voltage and reference DC voltage will contain opposite harmonic component.

$$V_{error} = V_{dc}^* - V_{dc} \quad \dots(9)$$

where  $V_{error}$  is difference between reference DC voltage ( $V_{dc}^*$ ), and APF reference DC bus voltage ( $V_{dc}$ ). In APF,  $V_{error}$  contributes reactive power required by load and compensating harmonic voltage. If  $V_{error}$  is considered a correction for inverter amplitude modulation index, actual index becomes

$$m_{actual} = \frac{V_{error} * V_{reference}}{V_{triangle}} \quad \dots(10)$$

Therefore, Eq. (8) becomes

$$V_{out} = m_{actual} * V_{dc} \quad \dots(11)$$

Eq. (11) shows that amplitude modulation index is dominating factor for APF.

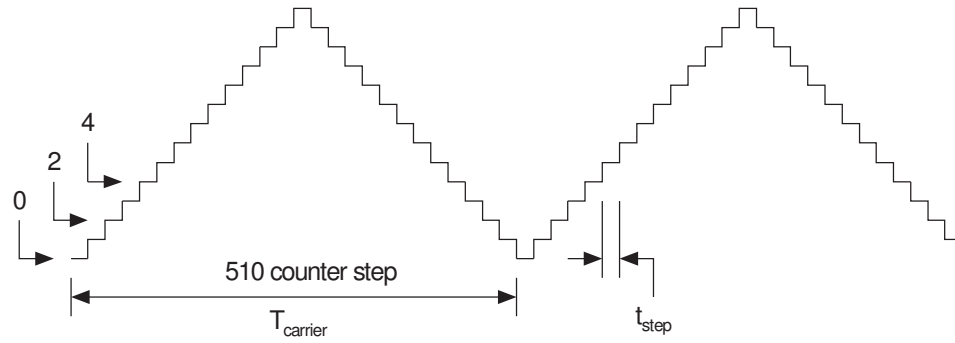


Fig. 3—Pattern of a carrier wave

Control of APF is digitally implemented in an Altera® FLEX 10K FPGA. Real-time generation of a sine wave through FPGA is time consuming. It is, therefore, inappropriate in PWM applications to calculate modulating wave values, which are required in 'real time'. An alternative approach is to store sine values in look-up table, which is programmed in permanent memory. Sine values are calculated first by this method. Memory requirements, operation efficiency, and output waveform accuracy depend on the number of samples defining a sine-wave cycle and their resolution. Higher gain, from over-modulation, is possible when compared with conventional PWM scheme<sup>8,10</sup>.

A sine voltage equation generates data to be stored in a ROM for sinusoidal waveform. Data (49 points) are generated for 90° (quarter cycle) of a sine waveform. An up-down counter reads ROM data. Each counting value determines each data's ROM address. it counts in up-count mode (0-48), and in down-count mode (47-01). Thus, 96 points represents one complete half cycle. If previous cycle were considered a positive half cycle, in negative half cycle the same data is counted continuously and separated by digital-AND technique.

Determination of carrier frequency ( $f_c$ ), decided to be 19.2 kHz, is based on inverter topology, acoustic radiations, type of power-switching devices used, and limitation of peripheral components. High-frequency operation is better than a low-frequency. However, at high frequency, switching stresses and power losses will increase<sup>11</sup>.  $f_c$  relates with main clock frequency and up-down counter as

$$f_c = \frac{f_{clk}}{(2^n - 1) * 2} \quad \dots(12)$$

where,  $f_{clk}$  is main clock frequency and  $n$  is bit size of up-down counter.

In triangle waveform, developed from an up-down counter and some peripheral logic gates, counter is clocked externally by a clock generated from phase locked loop circuit (Fig. 3).  $f_{clk}$  (9.83MHz) determines up-down counter's rate of increment or decrement. Fig. 4 shows every step of carrier wave. Data for sine wave is stored in an internal ROM with 49 points for a 90° modulating wave. For output data taken from ROM memory, counting time of up-down counter depends on PWM circuit design and on  $f_{clk}$ . All 96 points must be synchronized with 192 carrier waves and 10 ms operating time, i.e., half cycle (180°) of a sine wave. In its implementation, counter's clock must be fed with a correct  $f_{clk}$  for output designed.

Comparison between carrier and modulating signal must be done such that when carrier value is less or equal to modulating signal, PWM output level is HIGH, and when carrier value is more than modulating value, PWM output level is LOW. Comparison is done for every clock pulse in every counting step every 10 ms for carrier value, as well as for ROM data value. For a 4-switch bridge, two sets of out-of-phase pulses are needed. In order to develop two sets, PWM pulse train must be logical-AND with two sets of continuous ON and OFF pulses (10 ms) exactly opposite in phase, synchronized in-phase with one complete cycle of up-down-counting ROM data. Pulses (10 ms) are developed by a frequency divider in PWM circuit (Fig. 5).

### Experimental Setup

An experimental set-up specification is as follows: source voltage (line-neutral), 110 V (rms); source frequency, 50 Hz; source impedance inductance, 3 mH;

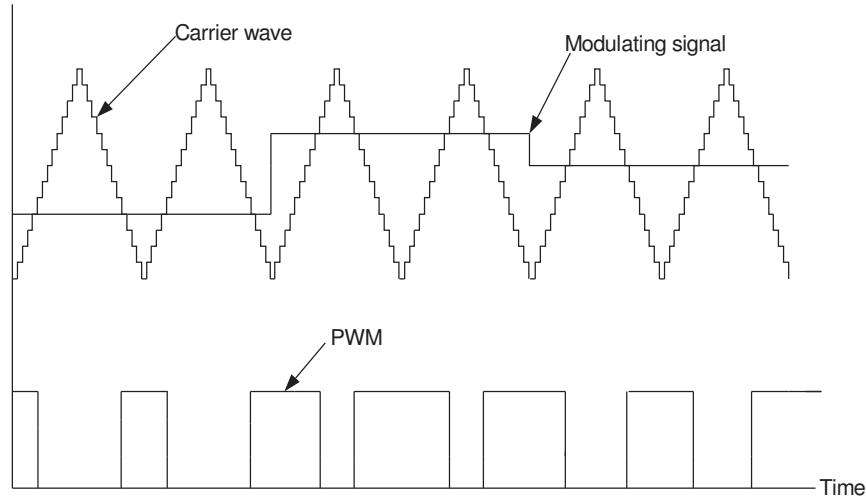


Fig. 4—Pulse generation technique

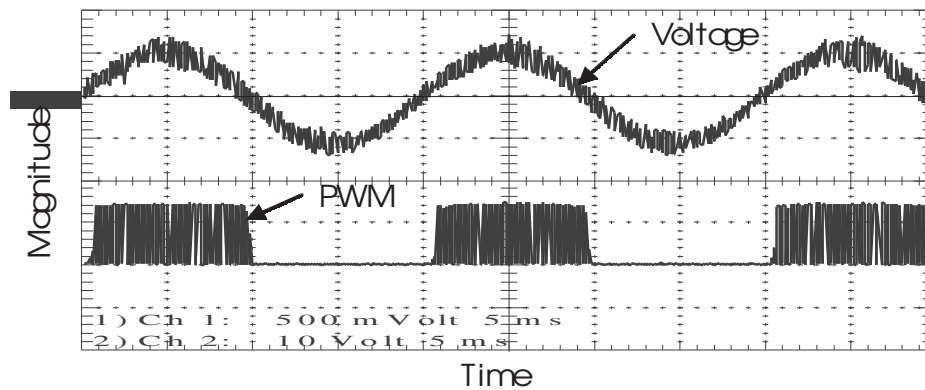


Fig. 5—PWM relative to system voltage

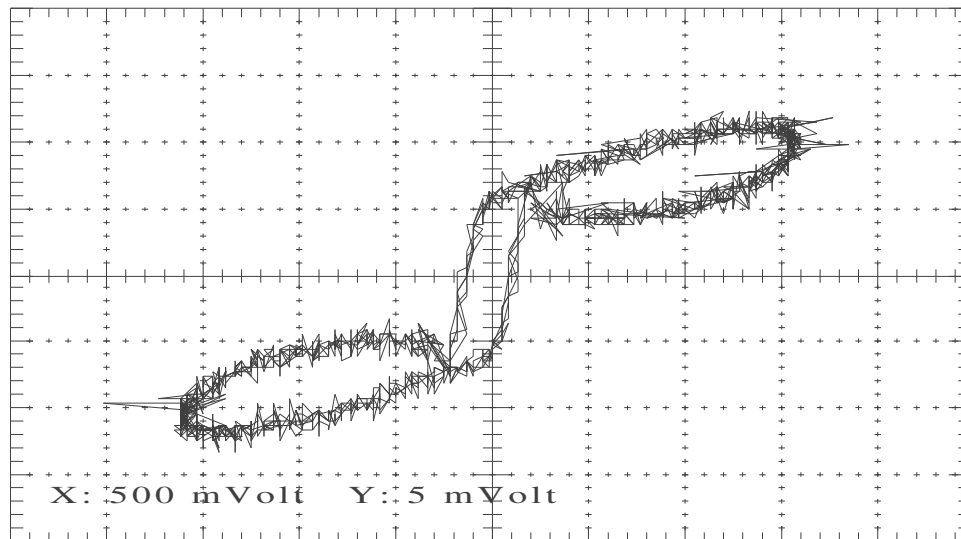
source impedance resistance,  $0.8 \, \Omega$ ; harmonic source inductance,  $200 \, \text{mH}$ ; harmonic source resistance,  $100 \, \Omega$ . Source voltage waveform is detected from source end before active and passive filter by using isolation amplifier, and source current is detected at source end before active and passive filter by using current probe. Voltage-measuring scale is selected from isolation amplifier setting and oscilloscope voltage scale, and current from current probe setting and oscilloscope voltage scale.

Oscilloscope data was transferred to computer using RS 232 port of oscilloscope. All data was exported in computer by using Wavestar software®, which was also used to analyze data in different mode (harmonic spectrum, individual harmonic component, total harmonic distortion, phase displacement, XY plot

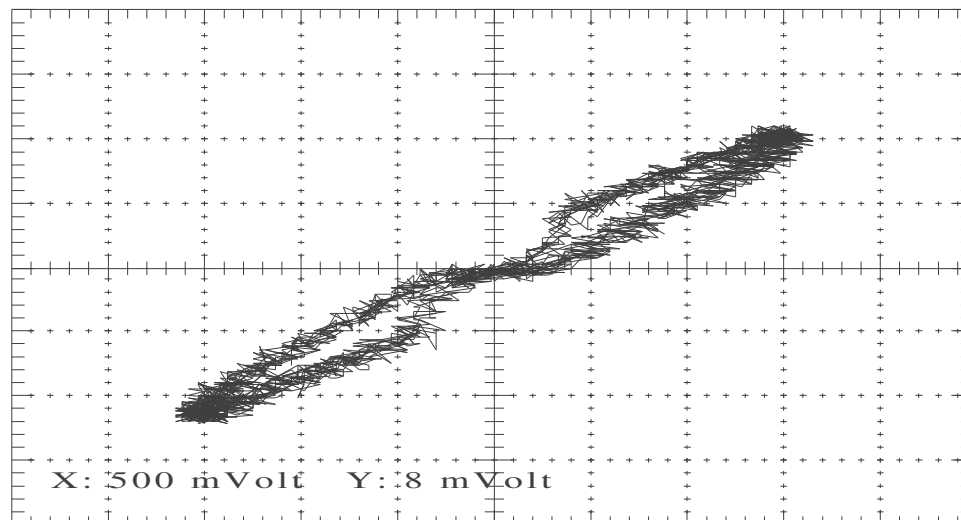
and power factor). Series connected APF specification is as follows: AC side low pass filter (resistance,  $0.8 \, \Omega$ ; inductance,  $2.5 \, \text{mH}$ ; capacitance,  $0.01 \, \mu\text{H}$ ); switching frequency,  $19.2 \, \text{kHz}$ ; transformer coefficient,  $0.5$ ; DC side capacitor,  $400 \, \mu\text{F}$ ,  $400 \, \text{V}$ ; snubber value (resistance,  $10 \, \Omega$ ; capacitance,  $0.01 \, \mu\text{F}$ ,  $1000 \, \text{V}$ ).

For comparison, harmonic contents of source currents before and after compensation are as follows: harmonics before compensation ( $3^{\text{rd}}$ ,  $15.89\%$ ;  $5^{\text{th}}$ ,  $10.46\%$ ;  $7^{\text{th}}$ ,  $3.27\%$ ;  $9^{\text{th}}$ ,  $2.85\%$ ); and harmonics after compensation ( $3^{\text{rd}}$ ,  $3.63\%$ ;  $5^{\text{th}}$ ,  $2.64\%$ ;  $7^{\text{th}}$ ,  $3.27\%$ ;  $9^{\text{th}}$ ,  $2.85\%$ ).

XY plot represents phase displacement and a rough idea about distortion of two waves (Fig. 6). If there is phase displacement between two waves, XY plot becomes elliptical, and without phase displacement



a)



b)

Fig. 6-XY plot of voltage and current source: a) before compensation; and b) after compensation

between waves, XY plot becomes a straight line of minimum distortion. For harmonic distorted wave, XY plot has no standard shape. From XY plot, phase displacement of two waves can also be measured.

### Conclusions

APF proposed can compensate current's harmonic components and reactive power while satisfying specifications of EMC standard IEC 61000-3-2<sup>12</sup>. PWM design, placed in an ALTERA® FLEX 10K FPGA, is flexible in producing PWM patterns, whether lagging, leading, or in-phase with, the reference voltage signal. Overall system requires no external memory.

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